IN THE SPECIFICATION:

Replace the paragraph beginning at page 7, line 10 with:

B1

A constraint of timings between the clock trees "to delay an average value of delay values from the starting point to each of the flip-flops in the clock tree 1 from an average value of delay values from the starting point to each of the flip-flops in the clock tree 2 by 2 ns (when the starting point is the output pin of the PLL)".

IN THE CLAIMS:

Cancel claim 6 and replace the indicated claims with:

C1

1. (Twice Amended) A method of designing a semiconductor circuit having clock trees, the method comprising :

generating a netlist;

inserting a plurality of delay gates into said netlist;

placing said netlist to produce a circuit placement;

generating clock trees for said circuit placement that satisfy a timing constraint;

routing said netlist after generation of said clock trees;

manually adjusting skew between said clock trees by deleting some of said delay gates inserted based on the timing constraint between said clock trees;

examining the skew between clock trees;

determining whether the timing constraint is satisfied; and

making a minimum change in the placing and routing when said delay gates are inserted.

B2

C2

2. (Amended) The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes collectively placing a plurality of delay gates.

3. (Amended) The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes collectively placing a plurality of delay gates in a region free of lines, other than clock lines, and free of gates, other than delay gates, so that clock lines are not influenced by other lines.

4. (Twice Amended) The method of designing a semiconductor circuit according to claim 2, wherein in manually adjusting skew between trees, said delay gates at first and last stages among said delay gates inserted are not regarded as targets to be deleted.